REMARKS

Claims 2-8, 10-11, and 13-19 are now pending in the application. Applicants have not amended the claims. The preceding Claim Listing is being presented for the Examiner's convenience. The Examiner is respectfully requested to reconsider and withdraw the rejection(s) in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 103

The claims stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Murty (U.S. Pat. No. 4,544,868) in view of Heinkel et al. (U.S. Pat. No. 6,351,091). This rejection is respectfully traversed.

As will be described further below, independent claims 17, 18 and 19 define a particular type of sharing of a fixed DC current level that is not shown, taught or suggested by either Murty or Heinkel et al. The Examiner has ignored the claim language in each of these claims that is not shown, taught or suggested by these references.

Each of these claims requires that the sum of the current in the subsequent phase plus the current in the preceding phase is equal to the fixed current level during commutation. This is an express restriction in each of the independent claims 17, 18 and 19. The Examiner failed to address this restriction anywhere in the Office Action.

Murty does not even discuss overlapping the current during commutation. The sum of the current that is provided by Heinkel et al. to the overlapped phases during commutation is variable. It is not fixed as recited in claims 17, 18 and 19.

Applicants will illustrate the difference in operation between Heinkel and Applicant's invention during the transition – in other words, when the current is shared during overlapping periods. Since Murty does not address sharing current during the overlapping periods, Murty is not relevant to this discussion.

During the overlapping period, Applicants pointed out that Heinkel et al. will provide a varying current level to the two overlapping phases. In the example set forth in Applicants specification, the fixed bus current is 1mA. This is the current level that is provided to a single phase during the non-overlapping periods. This is also the current level (1 mA) that is provided to two phases during the overlapping periods. Therefore, the DC bus current remains at the constant level (e.g. 1mA) during the overlapping periods as well.

Initially the current in a first phase is 1 mA before the overlap period starts. After the overlap period starts, the current in the first phase may be reduced to 0.9 mA and the current in the second or next phase may be increased to 0.1 mA. At this point, the sum of the current is still approximately 1 mA.

As the decreasing first phase/increasing second phase current distribution trend continues, the first phase receives 0.8mA and the second phase receives 0.2mA, for a total current of 1 mA. As the overlapping period continues, the first phase may receive 0.7mA and the second phase may receive 0.3mA for a total current of 1 mA. Eventually the first phase receives 0.1 mA and the second phase receives 0.9 mA for a total current of 1 mA. Finally, the overlapping period ends and the first phase receives 0 mA and the second phase receives 1 mA for a total of 1mA.

As can be appreciated, other current values can be used so long as the total remains at the fixed DC bus current level during overlapping and non-overlapping periods. The fixed DC current level may change in operation but the same relationship holds. The transition may be linear or nonlinear as long as the total current is shared and remains equal to the fixed DC current level.

Heinkel et al. does not show teach or suggest a switching circuit, method or control module that maintains a sum of the current to first and second phases substantially equal to the fixed current level during overlapping periods.

The current that is provided to the phases is pulse width modulated in Heinkel et al. As can be seen in FIG. 4 of Heinkel et al. (set forth below), the two phases do not share the DC bus current as claimed such that the sum is equal to a fixed DC current level.

The overlap period starts at time A. Just after time A, the PWM ratio or duty cycle of the first phase is approximately 100% and the PWM ratio or duty cycle of the second phase is approximately 30%. Therefore, at time A the current at the first phase is approximately 1 mA (assuming 100% duty cycle = 1mA) and the current at the second phase is approximately 0.3 mA (assuming 100% duty cycle = 1mA) for a total current of 1.3 mA for the two overlapping phases.

At time B, the PWM ratio or duty cycle of the first phase is approximately 95% and the PWM ratio or duty cycle of the second phase is approximately 50%. Therefore, at time B the current at the first phase is approximately 0.95mA and the current at the second phase is approximately 0.5mA for a total current of 1.45 mA for the two overlapping phases. At time C, the PWM ratio or duty cycle of the first phase is

approximately 85% (or 0.85mA) and the PWM ratio or duty cycle of the second phase is approximately 90-95% (or 0.9mA) for a total current of 1.75 mA for the two phases. Therefore, the supply current varies significantly from at least 1.3 mA to 1.75 mA during the overlapping period. As was pointed out above, the current level of Applicant's invention remains constant during Applicant's overlapping period.

It is abundantly clear that the total current that is provided to the phases during the overlapping period in Heinkel is a variable current – not the fixed DC bus current that is recited in Claims 17, 18 and 19.

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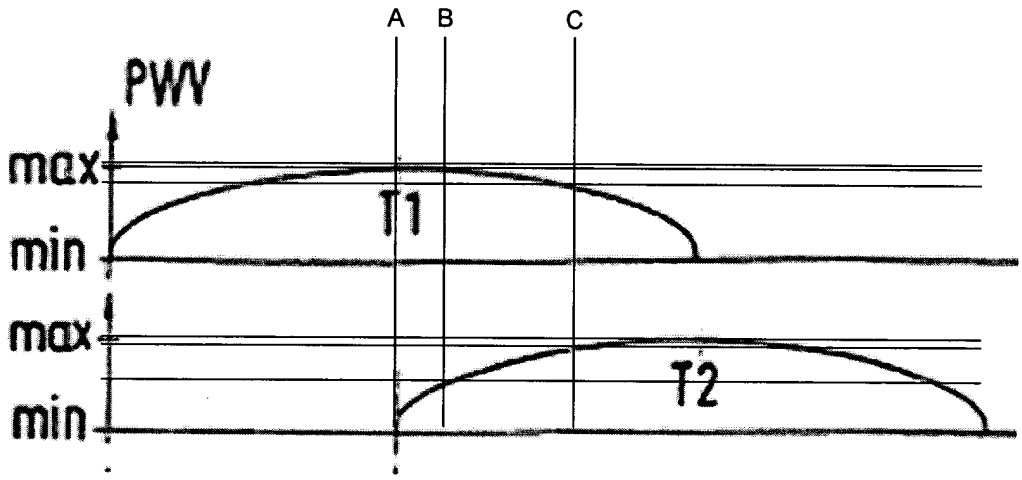

There does not appear to be any relationship between the current in the phases during the overlapping periods relative to a fixed DC level as set forth in the Claims 17-19.

In addition, it does not appear that the phases in Heinkel et al. ever have non-overlapping periods. In FIG. 4, T4 and T1 overlap. Then T1 and T2 overlap. Then T2 and T3 overlap. Then T3 and T4 overlap. Then the cycle repeats itself. Therefore,

Heinkel et al. does not have non-overlapping periods and fails to teach the non-overlapping periods required by claims 17, 18 and 19.

Based on the foregoing, Applicants believe that Claims 17-19 are allowable over the prior art of record. The remaining claims are either directly or indirectly dependent upon Claims 17-19 and are allowable for the same reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1211.

Respectfully submitted,

Dated: 10/16/03

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